

WHAT IS CLAIMED IS:

1. μ -law-to-A-law translating equipment, comprising:
 - a timing pulse generator that generates a reference frame pulse;
 - a μ -law signal receiving circuit that receives a μ -law PCM signal and outputs parallel μ -law PCM signals according to a reference frame pulse;
 - a multiplexer that time-division multiplexes plural parallel μ -law PCM signals and outputs a time-division multiplexed μ -law PCM signal;
 - a μ -law-to-A-law converter that converts the time-division multiplexed μ -law PCM signal to a time-division multiplexed A-law PCM signal;
 - a demultiplexer that demultiplexes the time-division multiplexed A-law PCM signal and outputs plural parallel A-law PCM signals; and
 - an A-law signal output circuit that receives the parallel A-law PCM signals and outputs a serial A-law PCM signal.

2. μ -law-to-A-law translating equipment according to Claim 1, comprising:
 - respective plural and the same number of μ -law signal receiving circuits and A-law signal output circuits.

3. μ -law-to-A-law translating equipment according to Claim 1, wherein:
 - the μ -law signal receiving circuit comprises:
 - a line receiver that converts a μ -law PCM signal from

5 bipolar to unipolar and outputs a unipolar μ -law signal;
6 a frame buffer that temporarily stores the unipolar μ
7 -law signal;
8 a frame detector that detects the frame leading part of
9 the unipolar μ -law signal and generates an address reset pulse
10 synchronized with the frame leading position for writing to the
11 frame buffer;
12 a frame position comparator that measures the time lag
13 in a position of a reference frame pulse and the address reset
14 pulse for writing to the frame buffer and generates an address
15 reset pulse for reading from the frame buffer; and
16 a serial-parallel converter that converts and outputs a
17 serial μ -law PCM signal read from the frame buffer to parallel
18 μ -law PCM signals.

1 4. μ -law-to-A-law translating equipment according to Claim
2 1, wherein:

3 the A-law signal output circuit comprises:
4 a parallel-serial converter that converts parallel A-
5 law PCM signals to a serial A-law PCM signal; and
6 a frame inserter that inserts a frame bit into the serial
7 A-law PCM signal.

1 5. μ -law-to-A-law translating equipment according to Claim
2 4, wherein:

3 the frame inserter inserts a frame bit according to a
4 reference frame pulse.

1 6. μ -law-to-A-law translating equipment according to Claim
2 4, wherein:

3 the A-law signal output circuit further comprises:

4 a line driver that outputs a serial A-law PCM signal at
5 a predetermined output amplitude level.

1 7. A-law-to- μ -law translating equipment, comprising:

2 a timing pulse generator that generates a reference frame
3 pulse;

4 an A-law signal receiving circuit that receives an A-
5 law PCM signal and outputs parallel A-law PCM signals according
6 to a reference frame pulse;

7 a multiplexer that time-division multiplexes plural
8 parallel A-law PCM signals and outputs a time-division
9 multiplexed A-law PCM signal;

10 an A-law-to- μ -law converter that converts the time-
11 division multiplexed A-law PCM signal to a time-division
12 multiplexed μ -law PCM signal;

13 a demultiplexer that demultiplexes the time-division
14 multiplexed μ -law PCM signal and outputs plural parallel μ -
15 law PCM signals; and

16 a μ -law signal output circuit that receives parallel
17 μ -law PCM signals and outputs a serial μ -law PCM signal.

1 8. A-law-to- μ -law translating equipment according to Claim
2 7, comprising:

3 respective plural and the same number of A-law signal
4 receiving circuits and μ -law signal output circuits.

1 9. A-law-to- μ -law translating equipment according to Claim
2 7, wherein:

3 the A-law signal receiving circuit comprises:

4 a line receiver that converts an A-law PCM signal from
5 bipolar to unipolar and outputs a unipolar A-law signal;

6 a frame buffer that temporarily stores the unipolar A-law
7 signal;

8 a frame detector that detects the frame leading part of
9 the unipolar A-law signal and generates an address reset pulse
10 synchronized with the frame leading position for writing to the
11 frame buffer;

12 a frame position comparator that measures the time lag
13 in a position of a reference frame pulse and the address reset
14 pulse for writing to the frame buffer and generates an address
15 reset pulse for reading from the frame buffer; and

16 a serial-parallel converter that converts a serial A-
17 law PCM signal read from the frame buffer to parallel A-law PCM
18 signals.

1 10. A-law-to- μ -law translating equipment according to Claim
2 7, wherein:

3 the μ -law signal output circuit comprises:

4 a parallel-serial converter that converts parallel μ -
5 law PCM signals to a serial μ -law PCM signal; and

6 a frame inserter that inserts a frame bit into the serial
7 μ -law PCM signal.

1 11. A-law-to- μ -law translating equipment according to Claim

2 10, wherein:

3 the frame inserter adds a frame bit to the serial μ -
4 law PCM signal according to a reference frame pulse.

1 12. A-law-to- μ -law translating equipment according to Claim
2 10, wherein:

3 the μ -law signal output circuit further comprises:
4 a line driver that outputs a serial μ -law PCM signal at
5 a predetermined output amplitude level.

1 13. μ -law-to-A-law and A-law-to- μ -law translating
2 equipment, comprising:

3 a timing pulse generator that generates a reference frame
4 pulse;

5 μ -law-to-A-law translating equipment; and

6 A-law-to- μ -law translating equipment, wherein:

7 the μ -law-to-A-law translating equipment comprises:

8 a μ -law signal receiving circuit that receives a μ -law
9 PCM signal and outputs parallel μ -law PCM signals according
10 to a reference frame pulse;

11 a multiplexer that time-division multiplexes plural
12 parallel μ -law PCM signals and outputs a time-division
13 multiplexed μ -law PCM signal;

14 a μ -law-to-A-law converter that converts the time-
15 division multiplexed μ -law PCM signal to a time-division
16 multiplexed A-law PCM signal;

17 a demultiplexer that demultiplexes the time-division
18 multiplexed A-law PCM signal and outputs plural parallel A-

19 law PCM signals;

20 an A-law signal output circuit that receives the parallel
21 A-law PCM signals and outputs a serial A-law PCM signal; and

22 the A-law-to- μ -law translating equipment comprises:

23 an A-law signal receiving circuit that receives an A-
24 law PCM signal and outputs parallel A-law PCM signals according
25 to a reference frame pulse;

26 a multiplexer that time-division multiplexes plural
27 parallel A-law PCM signals and outputs a time-division
28 multiplexed A-law PCM signal;

29 an A-law-to- μ -law converter that converts the time-
30 division multiplexed A-law PCM signal to a time-division
31 multiplexed μ -law PCM signal;

32 a demultiplexer that demultiplexes the time-division
33 multiplexed μ -law PCM signal and outputs plural parallel μ -
34 law PCM signals; and

35 a μ -law signal output circuit that receives the parallel
36 μ -law PCM signals and outputs a serial μ -law PCM signal.

1 14. μ -law-to-A-law and A-law-to- μ -law translating
2 equipment according to Claim 13, wherein:

3 the μ -law-to-A-law translating equipment comprises
4 respective plural and the same number of μ -law signal receiving
5 circuits and A-law signal output circuits; and

6 the A-law-to- μ -law translating equipment comprises
7 respective plural and the same number of A-law signal receiving
8 circuits and μ -law signal output circuits.